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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,400	06/28/2004	Hiroyuki Takahashi	UPM-02501	4403

7590 06/27/2005

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,400	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4-6,19 and 20 is/are rejected.

7)☒ Claim(s) 3 and 7-18 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 0804/.0904
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 09/22/2004.

Information Disclosure Statement (IDS) filed on 08/05/2004.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Regarding claim 1, line 11, should be changed "late write" to –late write writing control circuit writing—as defined in line 9--.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-2, 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Leung (U.S. Patent No. 6,415,353).

Regarding claim 1, Leung discloses a semiconductor memory device (Figure 5) having a memory cell array (1000-1127) comprised of memory cells requiring refresh, in which a read request or write request is asynchronously given for an access address, wherein the semiconductor memory device comprises:

a refresh timer (Figure 5, 302) periodically outputting a refresh request signal (RFREQ) for said memory cell array;

a late write writing control circuit writing (Figure 3, 100) , for said write request (WRQ#) an access address and write data for a write request given in a memory cycle before a memory cycle for the write request by late write (Column 12, lines 44-58); and

a refresh control circuit performing refresh for said memory cell array in response to the refresh request signal from said refresh timer, and delaying performance of said refresh a read operation or late write operation for a memory cell for the colliding read

request or write request is completed when said refresh request signal collides with said read request or said write request (Column 18, lines 21-67, Column 1-9, lines 1-5).

Regarding claim 2, Leung discloses wherein said refresh timer has a timer switching capability of setting a timer cycle during an active mode to be shorter than a timer cycle during a standby mode involving a refresh operation as a timer cycle in which its refresh request trigger is generated (Column 12, lines 60-67, Column 13, lines 1-55).

Regarding claims 4-6, Leung discloses a semiconductor memory device (Figure 3) having a memory cell array (200) comprised of memory cells requiring refresh, the semiconductor memory device comprising: a refresh request generator circuit (100) generating a refresh request independently of a read request or write request for said memory cells (Column 18, lines 14-20); and a refresh control circuit delaying performance of said refresh until a read operation or write operation for said memory cells for said read request or write request is completed when the refresh request from said refresh request generator circuit collides with said read request or write request (Column 2, lines 50-58, Column 4, lines 25-32, Column 12, lines 5-20), and wherein the write operation of performing said write operation is a late write operation of writing an access address and write data for a write request given in a memory cycle before a memory cycle for said write request (Column 12, lines 5-57), and further comprising an address storing apparatus (Figure 1, 184, 185, Column 7, lines 21-57) storing the present write request address, and an address hit control circuit making a comparison between the read request address and the write request address stored said address

storing apparatus at the time of the previous write request, and outputting an address hit signal when the former and the latter match each other (Column 3, lines 35-67, Column 4, lines 1-25) .

Regarding claims 19-20, the apparatus discussed above would perform the method claims 19-20.

Allowable Subject Matter

8. Claims 3, 7-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 7-18 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Leung (U.S. Patent No. 6,415,353), and others, does not teach the claimed invention having a refresh control pulse generator circuit having a capability of inputting a memory accessing enable signal, an address transition detection signal from a late write register storing memory access addresses, a refresh request trigger from said refresh timer and outputting a latch control signal controlling a latch operation of memory access addresses, a refresh address count-up signal, and a row enable normal signal and row enable refresh signal, and delaying the output of said row enable refresh signal until said latch control signal falls when the refresh request signal from said refresh timer is inputted during output of said latch control signal, and the semiconductor memory device has a page mode function, and is provided with the

address storing apparatus and the address hit control circuit for each of a page address and an address other than the page address.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER